REMARKS

Reconsideration of the application in view of the following remarks is respectfully requested.

The Examiner rejects claims 1, 2, 18, 19 under 35 U.S.C. 102(b) as being anticipated by Burns. The Examiner states that Burns discloses a successive approximation system and method, comprising as shown in Figure 5 a memory having a successive approximation value, and a comparison system 206 configured to amplify a difference between a test signal and a signal indicative of the successive approximation value to provide an amplified signal, and specifically refers to Col. 5, lines 23 – 30, and to convert the amplified signal to a digital signal and refers to Col. 5, lines 27-30. The Examiner also states that with respect to Claim 2, Burns discloses a successive approximation system further comprising a logic 218 to adjust the successive approximation value based on the digital signal shown in Figure 5.

This rejection is respectfully traversed. We agree that Burns shows a comparator 206 in Figure 5. The operation of this comparator is described in the portion of the text referred to by the Examiner in Col. 5. On lines 23 – 24 of Col. 5 it recites "The comparator 206 outputs one-bit comparator result signals to processor logic and memory circuit 218." (Emphasis added). Accordingly, it is clear that the comparator 206 is a well-known comparator circuit, which receives analog input signals and outputs a digital signal. Accordingly, the comparator 206 is not an amplifier.

In sharp contrast, the present invention utilizes a summer followed by an amplifier which is an input to an analog to digital converter. The circuit which most resembles Figure 5 of the reference is Figure 3 of the present application. In Figure 3, the input signal from the device under test is input to summation point 314 and summed with the reference signal output from the SAR DAC which is input to the summation point 314 and subtracted from the signal received from the device under test 304. The

output of the summation point is amplified by amplifier 320 and then converted to a digital signal by ADC 322. Thus, although the result is also a digital signal, the circuit contains the amplifier 320 whereas the circuit shown in Figure 5 of Burns contains no amplifier.

Original Claim 1 recites "a comparison system configured to amplify a difference between a test signal and a signal indicative of the successive approximation value", (Emphasis added) which is clearly not shown in Burns. Since the Examiner's rejection is an '102 rejection, the absence of this element means that the rejection must fail, the Examiner's statements to the contrary notwithstanding.

It should also be noted, that Burns does not suggest the utilization of an amplifier. The reason why the amplifier is needed is more clearly discussed in the background portion of the present application.

With respect to Claim 2, Claim 2 is dependent upon Claim 1 and is patentable for the same reasons.

With respect to Claim 18, it recites combining a test signal with a successive approximation signal, which is not shown in Burns. In Burns, the test generator 200 delivers a signal directly into the device under test. The only external signal that is received by the device 200 is the clock source 1, reference no. 208 which is not connected to any other portion of the circuit shown in Figure 5. Therefore, it clearly can not output a signal which is in any way related to the successive approximation signal.

With respect to Claim 19, this claim is dependent upon Claim 18 and patentable for the same reasons and, in addition, recites the amplification of the combined signal, which is not shown in Figure 5, as discussed above with respect to Claim 1.

The Examiner rejects claims 3 – 11 and 13 – 23, under 35 U.S.C. § 103(a) as being unpatentable over Burns. The Examiner states that with respect to claims 3 and 9, Burns discloses all of the limitations discussed above including a successive approximation system but does not explicitly disclose a successive approximation system, a comparison system further comprising a multi-bit analog to digital converter for converting the amplified signal to the digital signal, the multi-bit analog to digital converter having a range, the logic being responsive to adjust a successive approximation signal based on the digital signal to place the digital signal within the range of the multi-bit analog digital converter. The Examiner states that it is noted that in Burns the input signal may be analog or digital. The Examiner states that in applying a digital signal as the input of Burns, the artisan in the art would recognize that a ADC will provide a digital signal to Burns' circuit and Burns' circuit comprises a comparator 206 and a logic circuit 218. The Examiner concludes that it would have been obvious to one ordinary skill in the art at a time the invention was made that Burns' would achieve the same end result as the claimed invention performing successive approximation routines.

This rejection is respectfully traversed. First of all, Claim 3 recites a multi-bit analog to digital converter for converting the amplified signal to the digital signal. Claim 3 is dependent upon Claim 1 which recites the amplification, which as discussed above, is not shown or suggested by Burns. Therefore, Claim 3 is patentable for this reason alone. However, it should also be noted that Figure 5 of Burns shows a <u>one-bit</u> comparator 206, as clearly recited a Col. 5, line 24. (Emphasis added). Accordingly, comparing Claim 3 to the circuit shown as Figure 5 of Burns, we see that Burns only provides a <u>one-bit</u> output from comparator 206 and shows no amplification so he can not supply an amplified signal to the analog digital converter and it would be of no use to provide a multi-bit analog digital converter because only a single bit signal would be received. Claim 9 is dependent upon Claim 6 and is therefore patentable for the same

reasons. Claim 13 is directly dependent upon Claim 3 and is therefore patentable for the same reasons.

With respect to Claim 14, Burns does not show or suggest means for amplifying the different signal which as been discussed above with respect to Claim 1. The Examiner's statements to the contrary notwithstanding. In addition, Burns does not show or suggest utilization of a multi-bit digital comparison signal after the amplifier, first because it does not show the amplifier and second because the comparator 206 provides a single-big output signal, as discussed above.

The claims not specifically discussed are dependent upon claims which have been discussed and are therefore patentable for the same reasons.

Accordingly, Applicants believe the Application, as originally filed, is in condition for allowance, and such action is respectfully requested.

Respectfully submitted,

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